REMARKS

This amendment corrects errors in the text. Entry is respectfully solicited. This amendment is submitted prior to or concurrently with the payment of the issue fee and, therefore, no petition or fee is required. No new matter has been added.

Respectfully submitted,

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Date: December 3, 2002

BBJ/df:hlg:djp
Enclosures: Version of Specification with markings to show changes made
Version of Claims with markings to show changes made

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VERSION OF SPECIFICATION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please replace paragraph number **[0020]** with the following:

[0020] During normal operation, the buffer enable bank 105 is disabled for the first test mode and enabled for normal operation by the test mode signal having the second logic state at node 118 in order that user data can be driven from nodes 95 through the buffer enable bank 105 and the input/output buffer 80 to [110]pins 70, 126, 127, or 128.

VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (Amended) A load board interface, comprising:

a plurality of sets of interface nodes, each interface node of each of said plurality of sets of interface nodes configured to connect to corresponding input/output nodes of a semiconductor integrated circuit;

one set of tester nodes, each tester node of said one set of tester nodes configured to connect to one test station of a memory component tester; and

a switching structure [

]for electrically connecting each tester node of said one set of tester nodes to a [

]corresponding one of said interface nodes of each of said sets of interface nodes, and [

]for electrically connecting at least one interface node of each of said sets of interface[

]nodes to a corresponding one of said tester nodes.